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Metal Deposition and Front End Products

December 1, 2009

Applied Vantage® Astra™ DSA System

SIMPLY BETTER ANNEAL

APPLIED MATERIALS.

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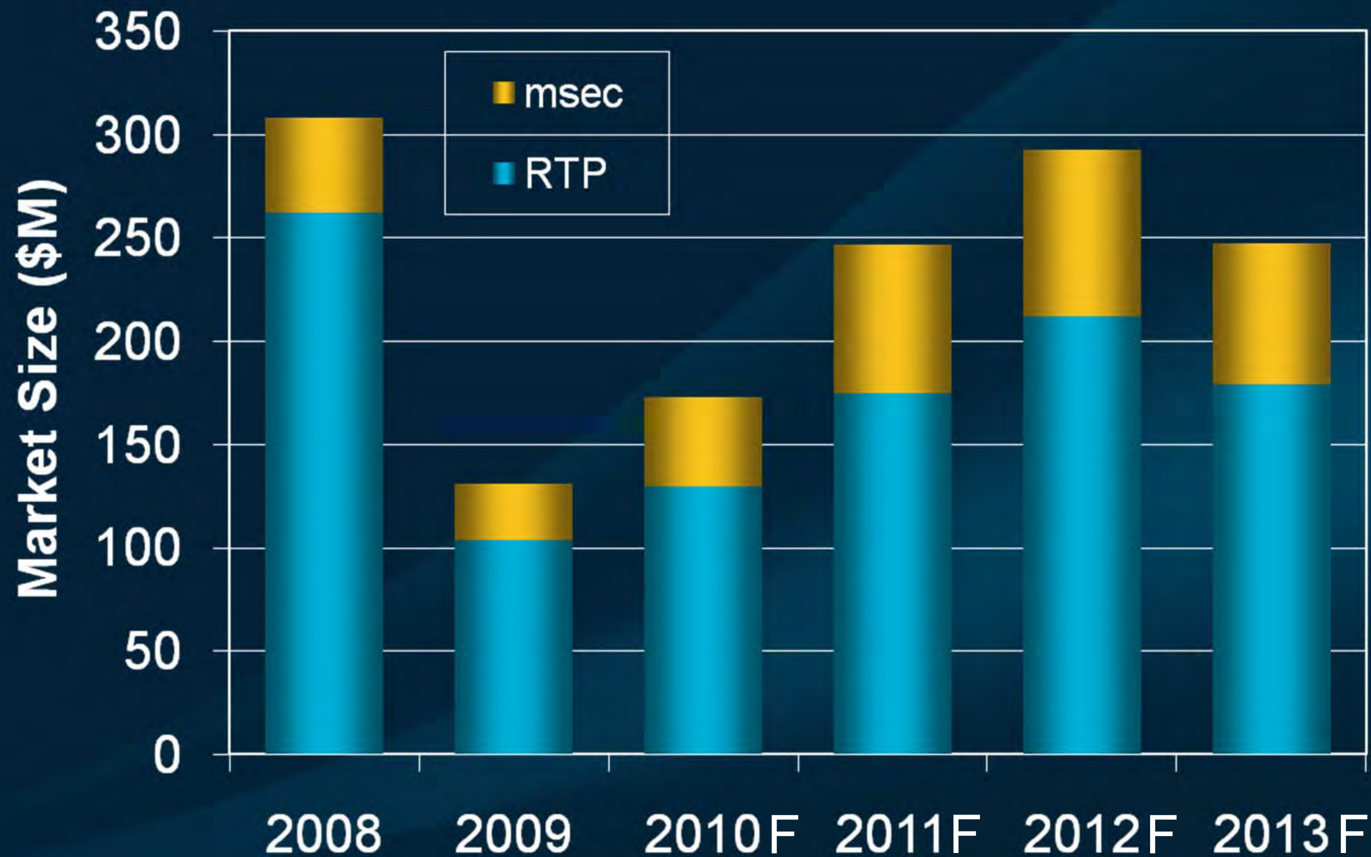
Rapid Thermal Processing Market Landscape



Source: Gartner Dataquest, September 2009

Millisecond anneals becoming a growing portion of SAM

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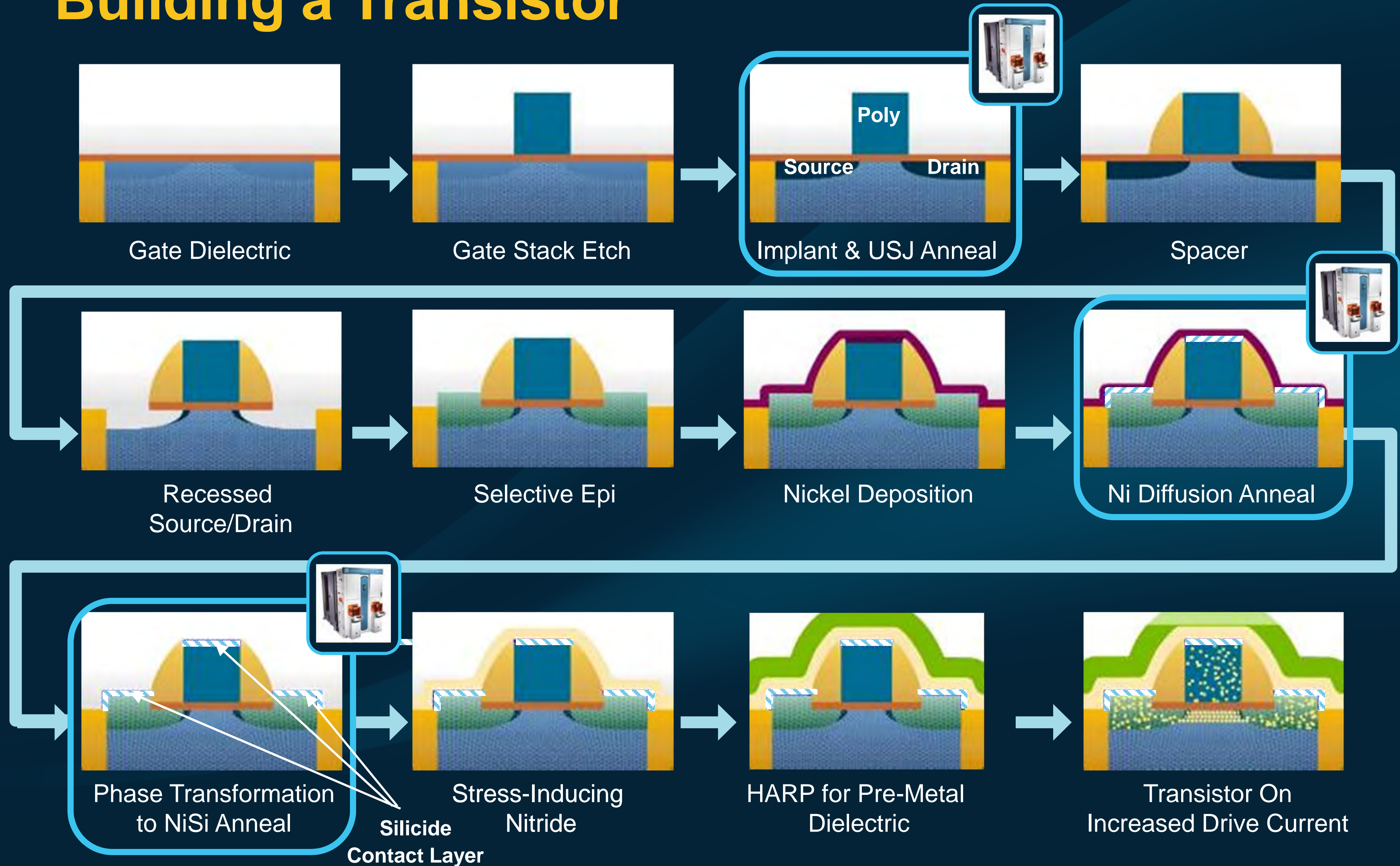
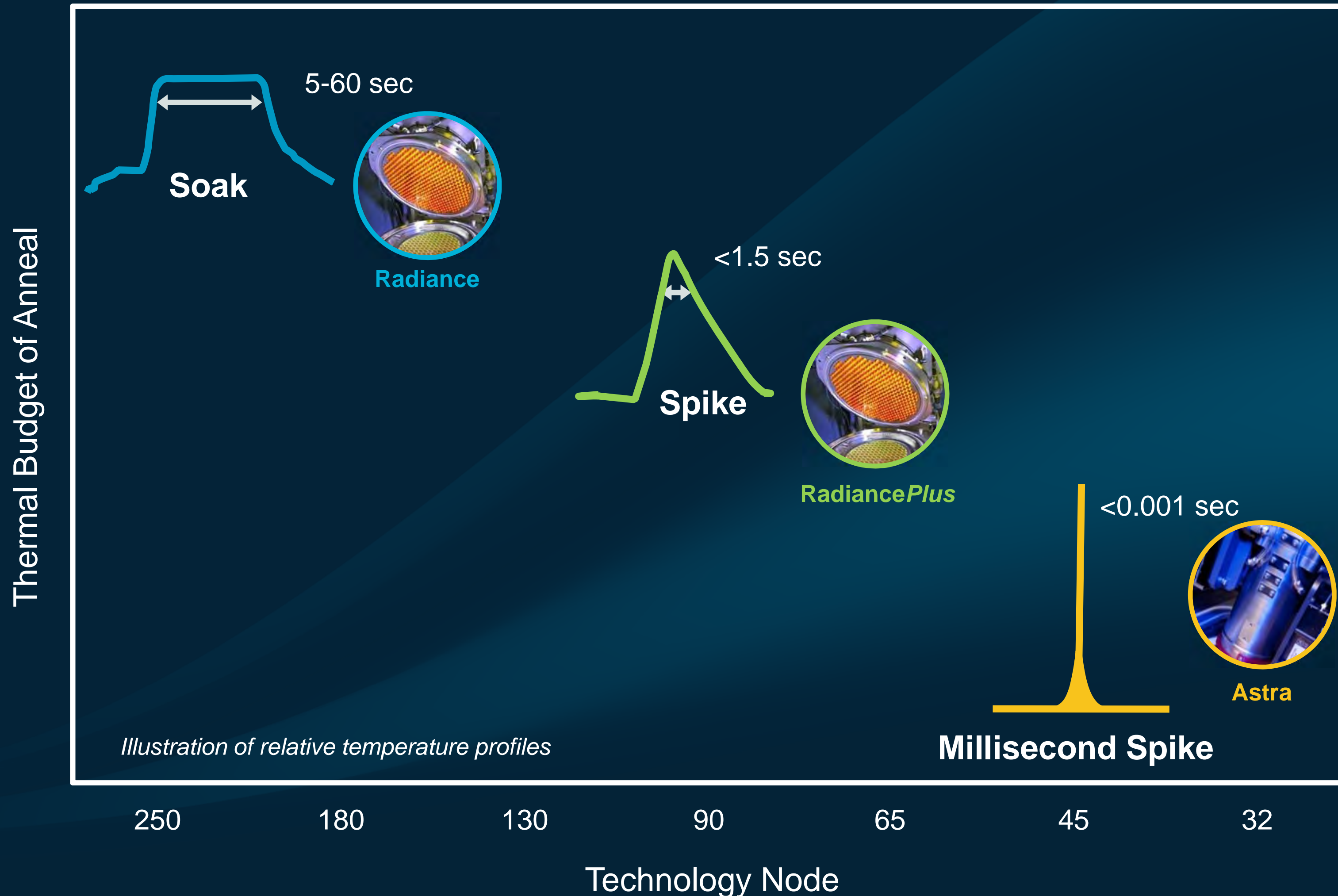
Building a Transistor



Anneal steps are key to device scaling

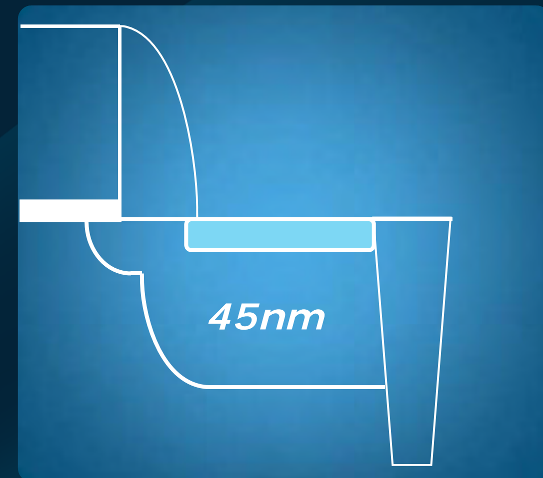
Evolution of Single-Wafer Anneals



Benchmark performance, consistently delivered by Applied Materials

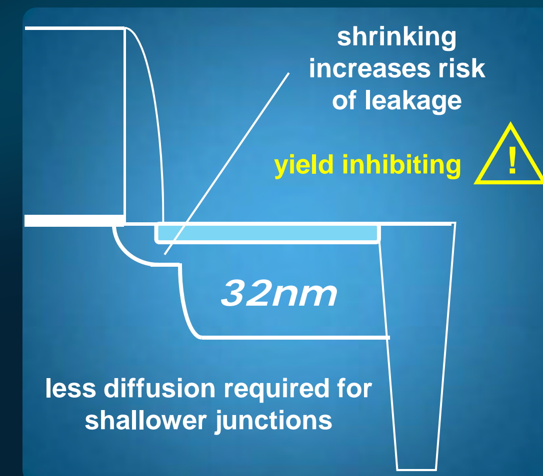
Annealing Technology Drivers

- **Transistor Scaling**
  - Minimized diffusion for shallower junctions
  - High dopant activation
  - Thinning nickel silicide contact layers
  - Avoiding yield-inhibiting piping defects



Future Applications

- **High-k/Metal Gate**
  - Work function optimization
- **Memory Yield Enhancements**
  - Minimizing defects in cell array
  - Applying logic junction engineering advances to periphery
- **3D Devices**



Improved silicide contact is key to scaling without degrading leakage

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Building a Transistor

Gate Dielectric

Gate Stack Etch

Implant & USJ Anneal

Spacer

Recessed Source/Drain

Selective Epi

Nickel Deposition

Ni Diffusion Anneal

Phase Transformation to NiSi Anneal

Stress-Inducing Nitride

HARP for Pre-Metal Dielectric

Transistor On Increased Drive Current

Millisecond Soak or Spike

Advanced anneals are key to scaling

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Trend toward Millisecond Anneal

	Main Anneal Steps in FEOL Flow	Logic (65nm) Poly Gate	Logic (45nm) Poly Gate	Logic (32nm) Hi-k Metal Gate
	Pre Gate Anneals	Soak	Soak	Soak
USJ	Source-Drain-Poly Implant Activation and Diffusion	Spike	Spike	Spike
USJ	Activation Boost		Millisecond	Millisecond
USJ	HKMG Work-Function Optimization Anneal			Millisecond
NiSi	Ni Silicidation Diffusion	Soak	Soak	Soak or Millisecond
NiSi	NiSi Phase Transformation	Soak	Soak or Millisecond	Millisecond

similar use of millisecond can be made in DRAM periphery

Need higher activation temperature, improved leakage control, shorter dwell time

Trend toward Millisecond Anneal

Main Anneal Steps in FEOL Flow	Logic (65nm) Poly Gate	Logic (45nm) Poly Gate	Logic (32nm) Hi-k Metal Gate
Pre Gate Anneals	**Soak**	**Soak**	**Soak**

USJ

Spike to Millisecond

Lower spike temperatures reduce activation in ultra-shallow junctions; need diffusion-less boost

Millisecond Delivers :

- Thinner effective gate oxide at temperatures >1150°C
- Added source-drain activation without added diffusion
- Minimal impact on limited thermal budget

NiSi

Soak to Millisecond

Thinner silicides without comprising conductivity or yield

Millisecond Delivers :

- Improved dopant activation at higher temperature
- Super-fast ramp up/down without deactivation typical of long exposures at mid-range temps
- Fewer leakage-inducing defects through steep temperature profile

Nickel silicidation is the most challenging millisecond anneal

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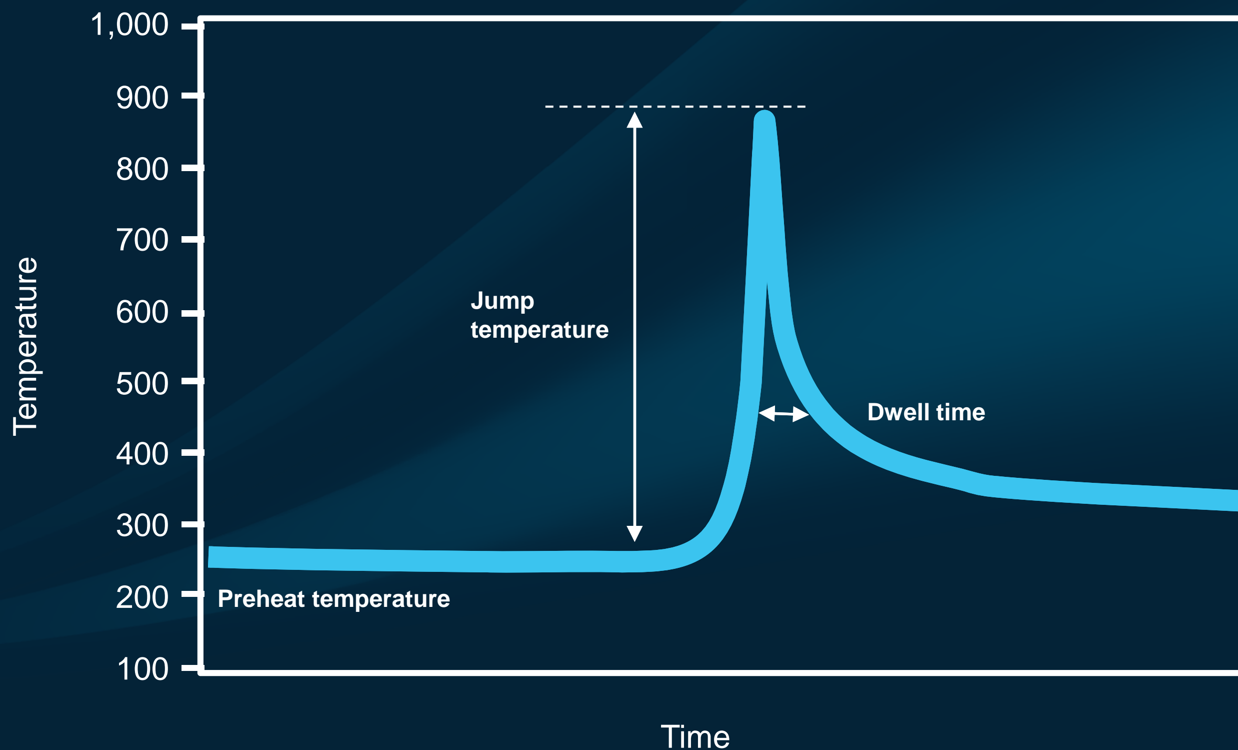
The Ideal Time-Temperature Profile for NiSi

Key parameters to consider

Preheat : Must be low enough to avoid uncontrolled diffusion

Jump temp : Must be high enough to enable optimal activation w/o wafer breakage or agglomeration

Dwell time : Must be short to avoid wafer bow and breakage



Above profile is key to enabling optimal nickel silicide

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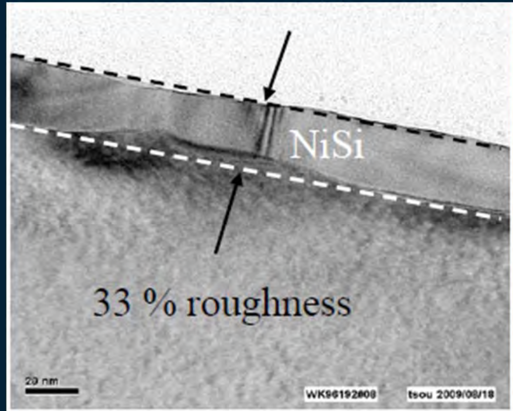
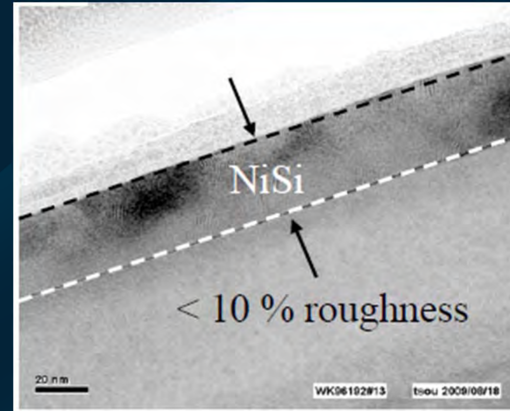
NiSi Morphology Improvement



RTP-1 anneal: T1 Soak
RTP-2 anneal: T2 Soak



RTP-1 anneal: T1-40ºC Soak
RTP-2 anneal: T2+400ºC Millisecond

Source: IEEE - RTP2009 Conference, *Advances on 32nm NiPt Salicide Process*, Dr. Chen et al. Co-published by UMC / Applied Materials

Lowest interface roughness achieved with reduced RTP-1 soak temperature and millisecond RTP-2

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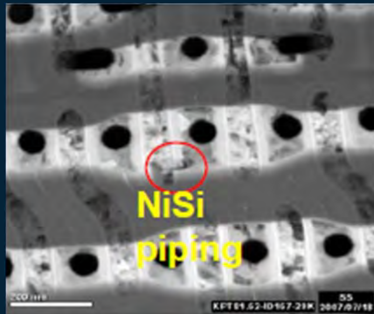
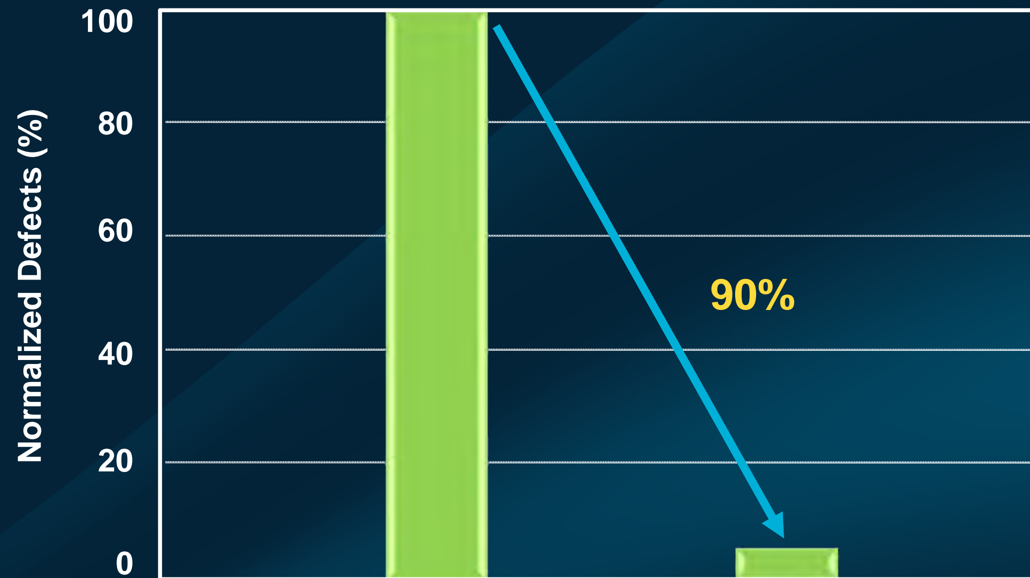
NiSi Piping Defects Reduction

TEM Top View



Piping Defects Count



RTP-1 anneal:	T1 Soak	T1-40ºC Soak
RTP-2 anneal:	T2 Soak	T2+400ºC Millisecond

Based on e-beam Bright Voltage Contrast (BVC) count on a pattern wafer post WCMP

Source: IEEE - RTP2009 Conference, *Advances on 32nm NiPt Salicide Process*,
Dr. Chen et al. Co-published by UMC / Applied Materials

Lowest piping defects count achieved with combination of reduced RTP-1 soak temperature and millisecond RTP-2

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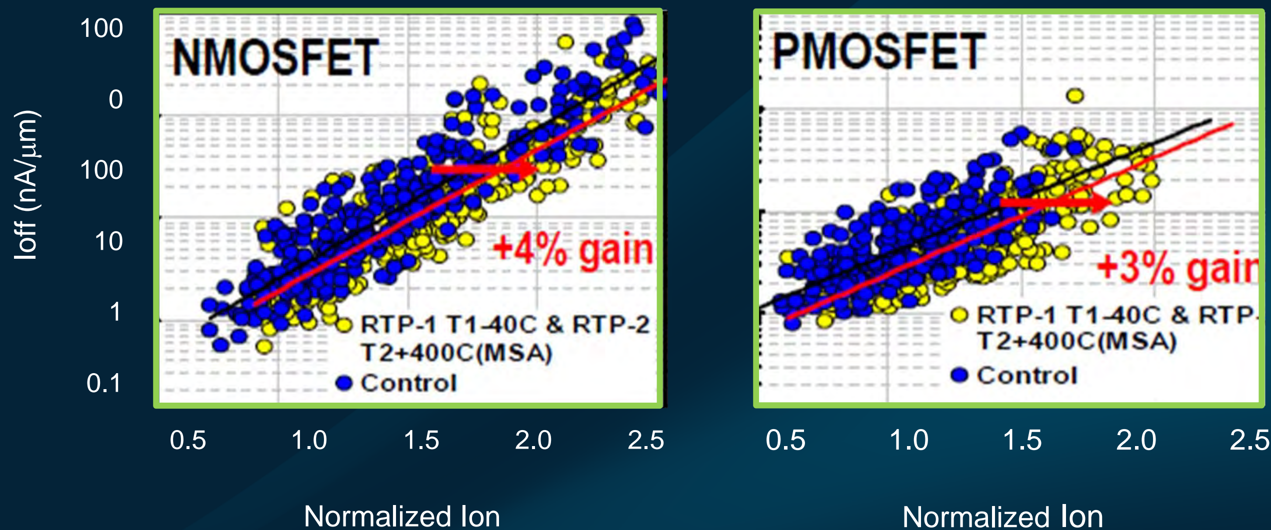
Electrical Performance – I_{on}/I_{off}

RTP-1: Soak @ T1-40ºC
RTP-2: Millisecond (T2+400ºC)



NMOS gain = 4% PMOS gain = 3%

Source: IEEE - RTP2009 Conference, *Advances on 32nm NiPt Salicide Process*, Dr. Chen et al. Co-published by UMC / Applied Materials

Several percent drive current gain achieved by enhancing nickel silicide contact using millisecond annealing with low temperature RTP-1 soak

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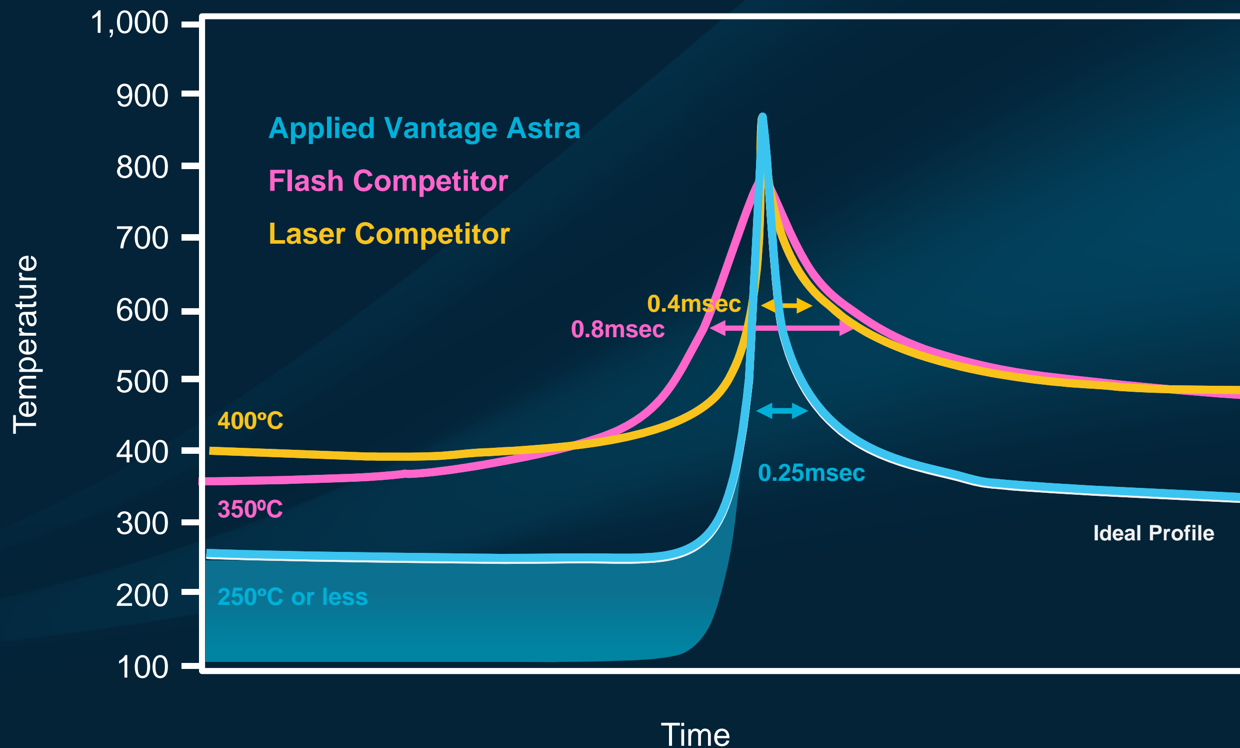

Delivered by Applied Materials' Vantage Astra system

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Applied Vantage® Astra™ DSA System

- **Uniquely powerful silicidation**
  - Up to 5% greater device speed
  - Higher yields enabled by up to 15x lower leakage
  - Less wafer stress
- **Versatile dynamic millisecond anneal**
  - Broad range of processing conditions
  - Ambient control
  - Extendible to high-k/metal gate applications
- **Compact, reliable, cost-effective**
  - Simple, compact and smart chamber design
  - Solid-state laser with prolonged lifetime
  - > 40 WPH per two- chamber system
  - Compatible with an RTP chamber on same system as hybrid

FAST. SMART. RELIABLE.
Simply Better Anneal

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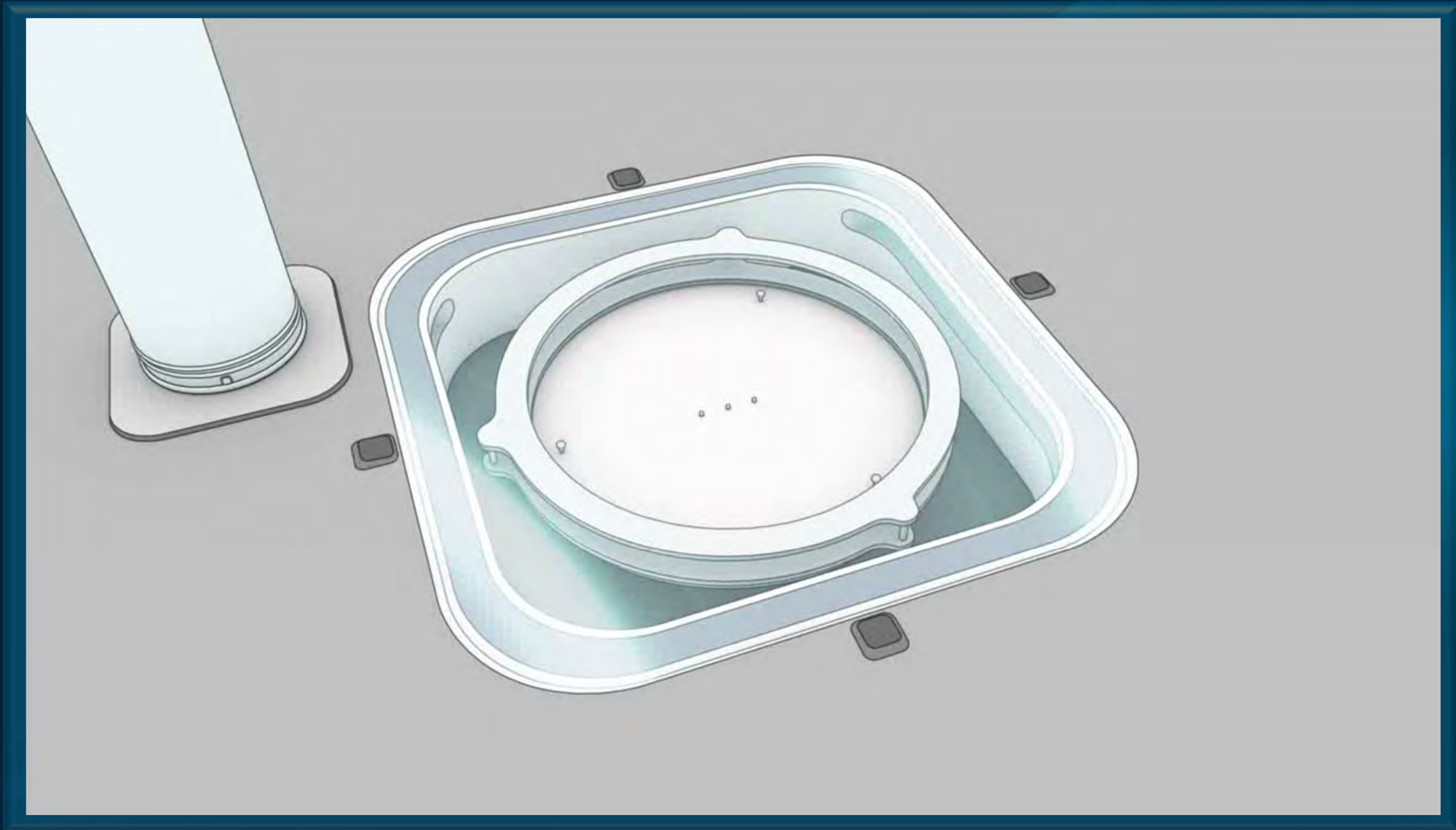
Applied Vantage Astra DSA System



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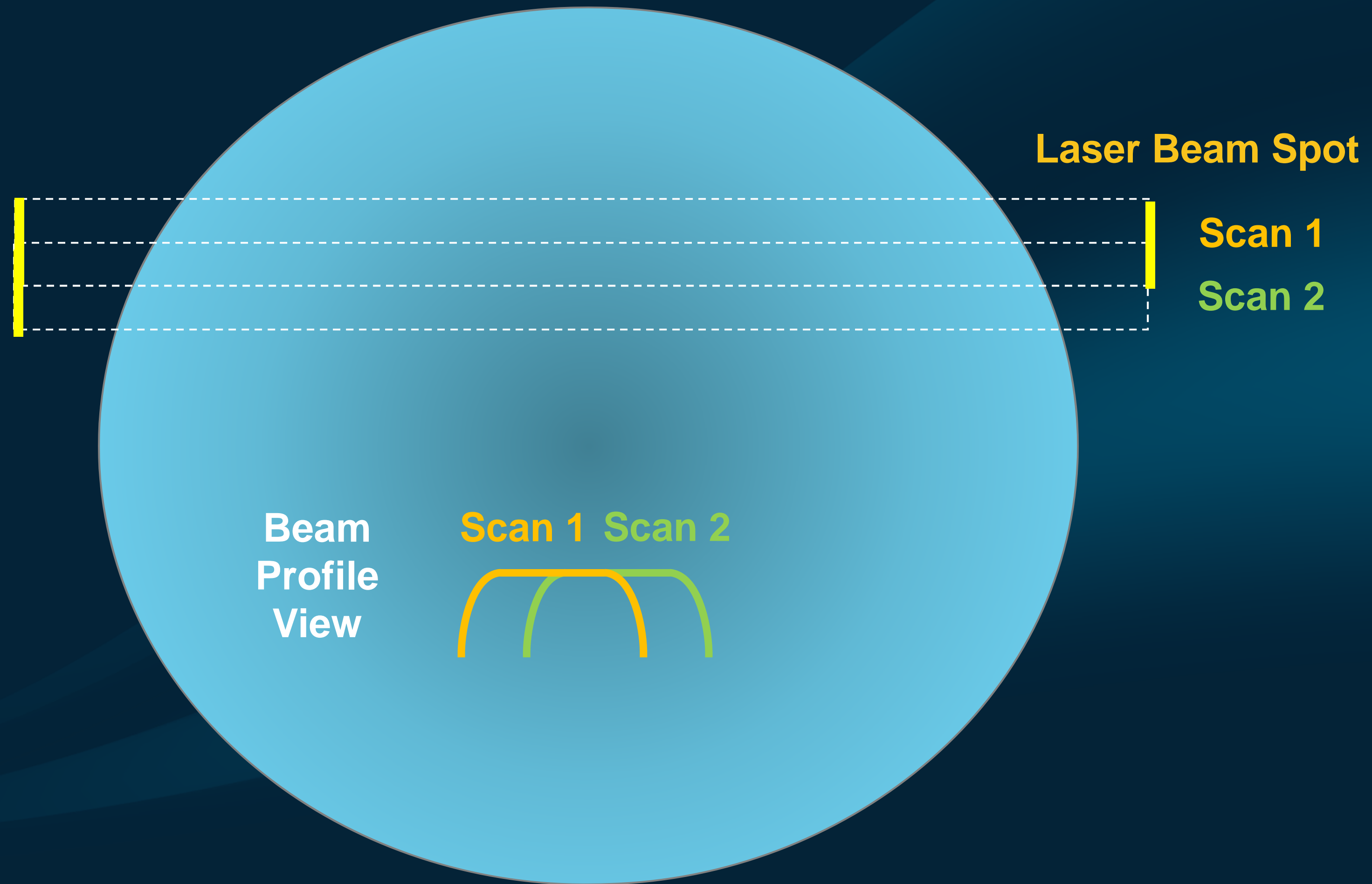
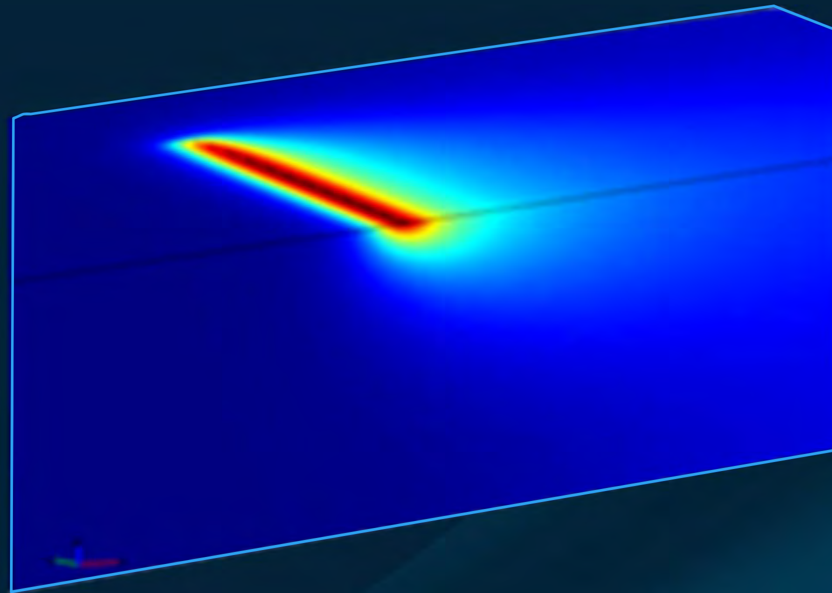
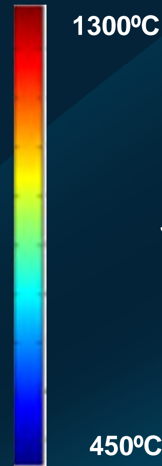
Scan and Overlap Concept

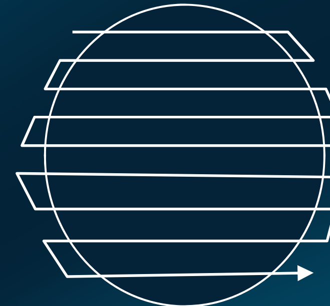


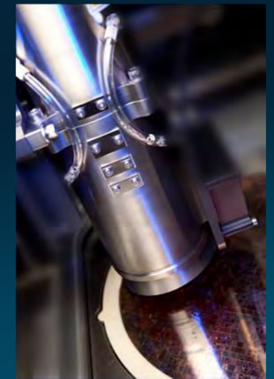
Dynamic Surface Annealing (DSA)

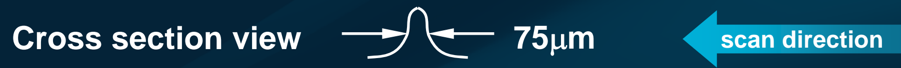
Three dimensional steady state result for 810nm







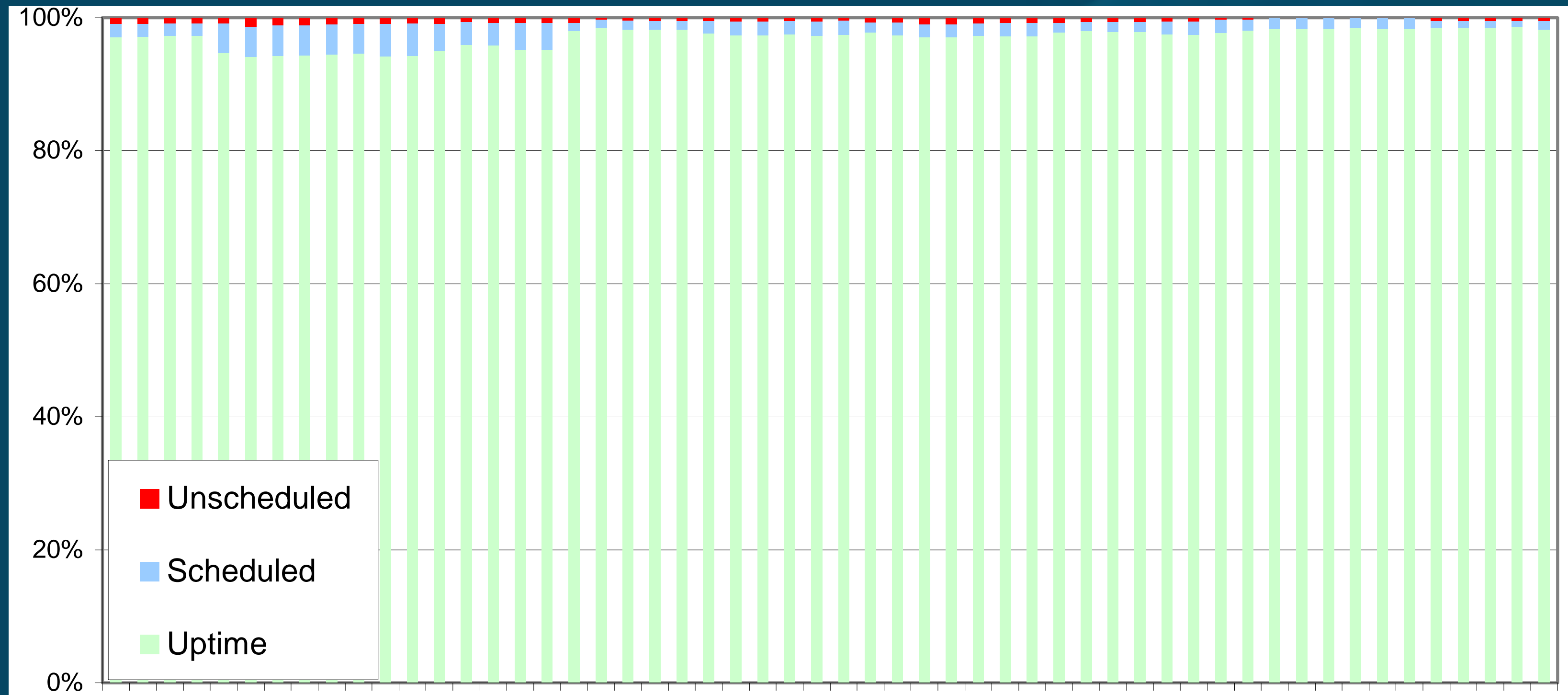




Simulation results on bare silicon

Modifying scan speed determines anneal dwell (exposure) time

Availability



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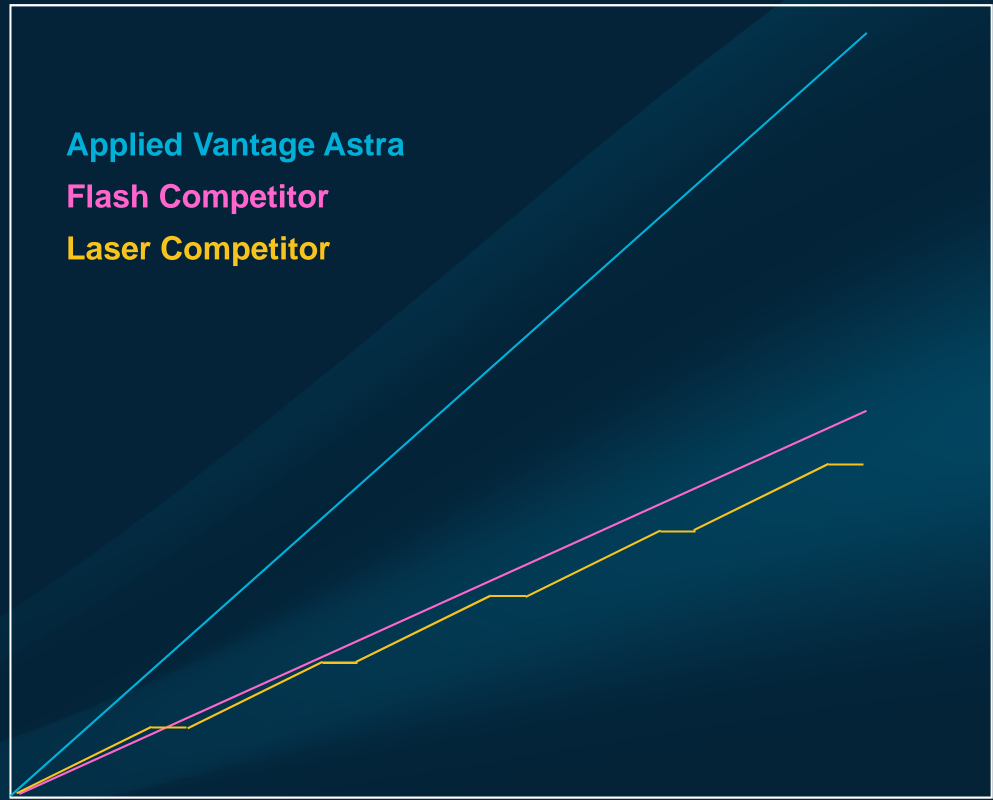
Productivity: Competitor Comparisons



FAST. SMART. RELIABLE.

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Applied Vantage Astra DSA System

- **FAST**
  - Higher throughput
  - Shorter dwell time
- **SMART**
  - Compact design
  - Broad process window
  - Ambient control
- **RELIABLE**
  - Solid-state laser
  - Reduced wafer stress
  - Based on the production proven Vantage

Simply Better Anneal

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